What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method for writing to a memory element, said method comprising:

precharging a conductor to a first voltage value, said first voltage being held on said conductor by a capacitance associated with said conductor;

coupling a programmable conductor memory element between said first voltage on said conductor and a second voltage to write a predetermined resistance state in said memory element.

2. A method as in claim 1 wherein said first voltage is higher than said second voltage to write a predetermined resistance state in said memory element.

3. A method as in claim 1 wherein said first voltage is lower than said second voltage to write a predetermined resistance state in said memory element,

4. A method as in claim 1 wherein said associated capacitance comprises a parasitic capacitance of said conductor.

5. A method as in claim 1 wherein said associated capacitance comprises a capacitor coupled to said conductor.

6. A method as in claim 1 wherein said associated capacitance comprises a parasitic capacitance of said conductor and a capacitor coupled to said conductor.

7. A method as in claim 1 wherein said programmable conductor memory element is coupled to said conductor by enabling an access transistor.

8. A method as in claim 2 wherein said first voltage is at or approximately at Vdd and said second voltage is Vdd/2.

9. A method as in claim 3 wherein said first voltage us ground and said second voltage is at or approximately at Vdd/2.

10. A method as in claim 1 wherein said conductor is a bit line associated with said memory element.

11. A method as in claim 1 wherein said memory element comprises a chalcogenide glass memory element.

12. A method as in claim 11 wherein said chalcogenide glass memory element comprises a germanium:selenium glass composition which is doped with silver.

13. A method for writing a semiconductor memory cell, the method comprising:

applying a first predetermined voltage to a first terminal of a programmable conductor memory element;

charging a bit line of a memory array to which said memory cell belongs to a second predetermined voltage, said bit line having a parasitic capacitance which stores said second predetermined voltage;

applying a third predetermined voltage to a gate of a transistor to enable said transistor and couple said bit line to a second terminal of said programmable conductor memory element; and

using a voltage across said memory element when said transistor is enabled to establish a resistance state of said memory element.

14. The method of claim 13 wherein said second predetermined voltage is greater than said first predetermined voltage.

15. The method of claim 13 wherein said first predetermined voltage is greater than said second predetermined voltage.

16. The method of claim 13 wherein said voltage across said memory element is discharged through said memory element to establish said resistance state.

17. The method of claim 13 wherein said first predetermined voltage is at or approximately at Vdd/2 and said second predetermined voltage is at or approximately at Vdd.

18. The method of claim 13 wherein said first predetermined voltage is at or approximately at Vdd/2 and said second predetermined voltage is at or approximately at ground.

19. The method of claim 13 wherein said act of applying a first predetermined voltage comprises coupling a cell plate, to which said first terminal is coupled, to a source of said first predetermined voltage.

20. The method of claim 13 further comprising the step of selectively coupling at least one capacitor to said bit line to store said second predetermined voltage.

21. The method of claim 20 further comprising enabling a transistor to selectively couple at least one capacitor to said bit line.

22. The method of claim 13 wherein said parasitic capacitance has a value of about 500 fF.

23. The method of claim 13 wherein said programmable conductor memory element comprises a chalcogenide glass.

24. The method of claim 23 wherein said chalcogenide glass comprises a Ge:Se glass composition which is doped with silver.

25. A method of operating a memory cell, said method comprising:

precharging a bit line to a first voltage;

applying a second voltage to a first terminal of a chalcogenide memory element; and

connecting a second terminal of said chalcogenide memory element to said bit line to produce a voltage across said memory element sufficient to write a predetermined resistance state into said memory element.

26. The method of claim 25 wherein said second voltage is greater than said first voltage.

27. The method of claim 25 wherein said first voltage is greater than said second voltage.

28. The method of claim 25 wherein said first voltage is held on said bit line by a parasitic capacitance.

29. The method of claim 25 further comprising selectively coupling at least one capacitor to said bit line to receive and store said first voltage.

30. The method of claim 29 further comprising operating a transistor to selectively couple said at least one capacitor to said bit line.

31. The method of claim 25 wherein said bit line has a parasitic capacitance of about 500 fF.

32. The method of claim 25 wherein said chalcogenide memory element comprises a Ge:Se glass composition doped with silver.

33. The method of claim 25 wherein said connecting further comprises enabling a transistor to connect said second terminal to said bit line.

34. The method of claim 33 wherein said transistor is enabled by a word line voltage applied to a gate of said transistor.

35. A memory structure comprising:

a conductor having an associated capacitance;

a precharge circuit for precharging said conductor to a first voltage, said first voltage being held on said conductor by said associated capacitance;

a programmable conductor memory element having one terminal connected to a second voltage; and

an access device for selectively coupling a second terminal of said memory element to said conductor, said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state.

36. The memory structure of claim 35 wherein said access device is a transistor.

37. The memory structure of claim 35 wherein said precharge circuit supplies a first value as said first voltage to program a higher resistance state into said memory element and a second value as said first voltage to program a lower resistance state into said memory element.

38. The memory structure of claim 37 wherein said first value is at or approximately at Vdd, said second value is ground, and said second voltage is at or approximately at Vdd/2.

39. The memory structure of claim 35 wherein said associated capacitance comprises a parasitic capacitance of said conductor.

40. The memory structure of claim 35 wherein said associated capacitance comprises at least one capacitor coupled to said conductor.

41. The memory structure of claim 35 wherein said associated capacitance comprises a parasitic capacitance of said conductor and at least one capacitor coupled to said conductor.

42. The memory structure of claim 35 wherein said conductor is a bit line and said access device is enabled by a voltage applied to a word line.

43. The memory structure of claim 35 wherein said memory element comprises a chalcogenide glass memory element.

44. The memory structure of claim 43 wherein said chalcogenide glass memory element comprises a Ge:Se glass composition which is doped with silver.

45. A semiconductor memory comprising:

a bit line having an associated capacitance;

a programmable conductor memory element having first and second terminals;

a precharge circuit for precharging said bit line to one of two possible voltage values depending on a desired state of resistance programming of said memory element, said associated capacitance holding a precharge voltage value on said bit line;

a cell plate coupled to a first terminal of said memory element for supplying a third voltage value to said first terminal; and

an access transistor responsive to a voltage on a word line for selectively coupling said bit line to said second terminal of said memory element to program said memory element to a resistance state based on the voltage values on said cell plate and bit line.

46. The semiconductor memory of claim 45 wherein one of said two possible voltage values is higher than said third voltage value and the other of said two possible voltage values is lower than said third voltage value.

47. The semiconductor memory of claim 45 wherein said associated capacitance comprises a parasitic capacitance of said conductor.

48. The semiconductor memory of claim 45 wherein said associated capacitance comprises at least one capacitor coupled to said conductor.

49. The semiconductor memory of claim 45 wherein said associated capacitance comprises a parasitic capacitance of said conductor and at least one capacitor coupled to said conductor.

50. The semiconductor memory of claim 48 further comprising a switching device for selectively coupling said at least one capacitor to said bit line.

51. The semiconductor memory of claim 49 comprising a switching device for selectively coupling said at least one capacitor to said bit line.

52. The semiconductor memory of claim 45 wherein said memory element comprises a chalcogenide glass memory element.

53. The semiconductor memory of claim 52 wherein said chalcogenide glass memory element comprises a Ge:Se glass composition which is doped with silver.

54. The memory of claim 47 wherein said parasitic capacitance has a value of about 500 fF.

55. A memory cell comprising:

a chalcogenide memory element having first and second terminals;

a first memory line;

a circuit for selectively precharging said first memory line to either a first or second voltage;

a circuit for supplying a third voltage to the first terminal of said chalcogenide element; and

a device for switchably coupling the second terminal of said chalcogenide memory element to said first memory line after said first memory line has been precharged, said device causing a voltage to be applied across said chalcogenide memory element sufficient o write one of two predetermined resistance states in said chalcogenide element depending on which of said first or second voltage is precharged on said memory line.

56. The memory cell of claim 55 wherein said third voltage is between said first and second voltages.

57. The memory cell of claim 55 wherein said memory line further comprises a parasitic capacitance for holding an applied precharge voltage.

58. The memory cell of claim 55 further comprising at least one capacitor coupled to said memory line to receive and hold said precharge voltage.

59. The memory cell of claim 58 further comprising a switching device for selectively coupling said at least one capacitor to said memory line.

60. The memory of claim 57 wherein said memory line has a parasitic capacitance of about 500 fF.

61. The memory of claim 55 wherein said chalcogenide memory element comprises a germanium:selenium glass composition which is doped with silver.

62. A processor system comprising:

a processor; and

a semiconductor memory coupled to said processor, said semiconductor memory comprising:

a conductor having an associated capacitance;

a precharge circuit for precharging said conductor to a first voltage, said first voltage being held on said conductor by said associated capacitance;

a programmable conductor memory element having one terminal connected to a second voltage; and

an access device for selectively coupling a second terminal of said memory element to said conductor, said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state.

63. The processor system of claim 62 wherein aid access device is a transistor.

64. The processor system of claim 62 wherein said precharge circuit supplies a first value as said first voltage to program a higher resistance state into said memory element and a second value as said first voltage to program a lower resistance state into said memory element.

65. The processor system of claim 64 wherein said first value is at or approximately at Vdd, said second value is at or approximately at ground, and said second voltage is at or approximately at Vdd/2.

66. The processor system of claim 62 wherein aid associated capacitance comprises a parasitic capacitance of said conductor.

67. The processor system of claim 62 wherein said associated capacitance comprises at least one capacitor coupled to said conductor.

68. The processor system of claim 62 wherein said associated capacitance comprises a parasitic capacitance of said conductor and at least one capacitor coupled to said conductor.

69. The processor system of claim 62 wherein said conductor is a bit line and said access device is enabled by a voltage applied to a word line.

70. The processor system of claim 62 wherein said memory element comprises a chalcogenide glass memory element.

71. The processor system of claim 70 wherein said chalcogenide glass memory element comprises a Ge:Se glass composition which is doped with silver.